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10/693,568

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IN THE UNITED STATES PATENT OFFICE

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Applicants: Patrick Lysaght et al.  
Assignee: Xilinx, Inc.  
Title: Method and Apparatus for Power Optimization During an Integrated Circuit Design Process  
Serial No.: 10/693,568 File Date: 10/24/2003  
Examiner: Naum B. Levin Art Unit: 2825  
Docket No.: X-1374 US Conf. No.: 1995

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AMENDMENT IN RESPONSE TO FINAL OFFICE ACTION

Dear Sir:

In response to the Final Office Action mailed from the Patent Office on June 8, 2006, please replace/substitute the following claims as indicated.

Amendments to the claims are reflected in the list of claims that begins on page 2 of this paper.

Remarks begin on page 7 of this paper.